

REMARKS

Claims 31-34, 36, 37, 39, 48, 49, 52-56, and 65-67 are pending. Claims 31 and 52 have been amended and claims 1-30, 35, 38, 40-47, 50, 51 and 57-64 have been canceled.

Reconsideration of the application is respectfully requested for the following reasons.

In the Office Action, the Examiner rejected claims 31-34, 36, 37, 39, 48-56, and 65-67 under 35 USC § 102(e) for being anticipated by the Smith patent. This rejection is traversed for the following reasons.

Claim 31 covers a semiconductor device having two sets of signal wires. The first set of signal wires includes a first plurality of wires in a first layer and a second plurality of wires in a second adjacent layer. The second set of signal wires includes a third plurality of wires in the first layer and a fourth plurality of wires in the second layer. The wires in the first and second sets are arranged in first and second patterns and are substantially parallel.

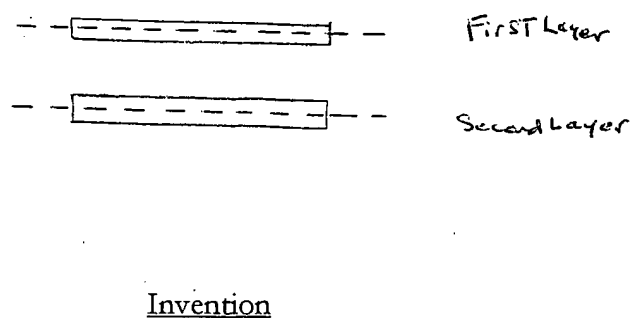
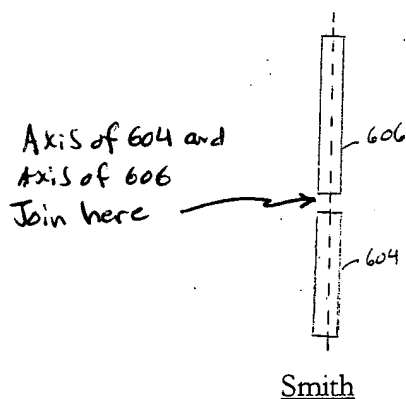
In addition to these features, claim 31 recites that “the first and second layers are on different vertical levels of said device” and that “the signal wires in the first layer and the signal wires in the second layer extend along different longitudinal axes which do not intersect.” These features are not disclosed by the Smith patent.

The Smith patent discloses a semiconductor device having a plurality of segments 604 and 606 which the Examiner has identified as signal wires. In rejecting claim 31, the Examiner provided an annotated diagram showing how it is believed Figure 6 of Smith includes the features of the invention. This diagram shows that the first and second layers reside side-by-side on the same horizontal surface of one layer (M7) of the device. This is evident from the disclosure in Smith that Figure 6 is a plan view, in contrast to Figure 1 which is described as a cross-sectional view.

By residing on layer M7, it is clear that all the segments 604 and 606 which the Examiner identified as corresponding to the signal wires in the first and second layers of the first and second sets of the invention reside on the same horizontal surface (M7) in one vertical layer of an integrated circuit device.

In contrast, Applicants' drawings provide cross-sectional views of the signal wires in the first and second layers. As these drawings and corresponding portions of the specification make clear, the first and second layers are on different vertical levels, not on a same horizontal surface as shown in Figure 6 of the Smith patent. To make these differences more evident, claim 31 has been amended to recite that "the first and second layers are on different vertical levels of said device." These features are not disclosed by the Smith patent.

Claim 31 further recites that "the signal wires in the first layer and the signal wires in the second layer extend along different longitudinal axes which do not intersect." Smith also fails to disclose these features. As shown in the annotated diagram of Figure 6 in the Office Action, the signal wires 604 and 606 in the first and second layers of each set are aligned along common longitudinal axes. Moreover, these axes intersect at areas where ends of signal wires 604 and 606 face one another as the following diagram indicates.



Claim 31 further recites that the device further includes “one or more ground or return wires that extend parallel to the signals wires in the first and second sets, the ground or return wires disposed between the signal wires in the first set and the signal wires in the second set.” While the Smith patent discloses the use of ground wires, they are not provided between the wires in the first and second sets in the manner recited in claim 31. Accordingly, the invention of claim 31 and the Smith patent are very different.

Because the Smith patent does not disclose all the features of claim 31, it is respectfully submitted that the Smith patent does not anticipate this claim. Applicants further submit that these differences are sufficient to render claim 31 non-obvious and thus patentable over Smith, and that the claims which depend from claim 31 are allowable not only by virtue of their dependency from claim 31 but also based on the features separately recited therein.

Claims 31, 53, 54, and 65-67 were rejected under 35 USC § 102(b) for being anticipated by the Koya patent. This rejection is traversed for the following reasons.

The Koya patent discloses a semiconductor device formed from two sets of signal wires. As shown in the annotated diagram of Figures 9 and 10 in the Office Action, the first set of signal wires is located on the left side of the Examiner’s dotted line and the second set of signal wires is located on the right wide of this dotted line. The Examiner further noted that layers 72 and 75 are ground layers.

However, ground layers 72 and 75 do not extend parallel to the signal wires in the first and second sets, as is required of the ground or return wires of claim 31. On the contrary, layers 72 and 75 are perpendicular to the signal wires (42, 73, 74, 84) in the first and second sets. Moreover, ground layers 72 and 75 are not disposed between the signal

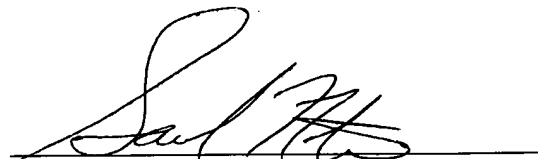
wires in the first set and the signal wires in the second set as is required of the ground or return wires of claim 31. Instead, layers 72 and 75 are disposed between the signal wires of each set, not between the signal wires in the first set and the signal wires in the second set.

Accordingly, it is apparent that claim 31 defines a semiconductor device having a structure very different from the structure disclosed in the Koya patent. It is respectfully submitted that claim 31 and its dependent claims are allowable over Koya based on at least these differences.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Withdrawal of the rejections in the Final Office Action and furtherance of the application to allowance is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with this application to Deposit Account No. 16-0607 and credit any excess fees to the same Deposit Account.

Respectfully submitted,



Attorneys for Intel Corporation

Mark L. Fleshner
Registration No. 34,596

Samuel W. Ntiros
Registration No. 39,318

FLESHNER & KIM, LLP
P.O. Box 221200
Chantilly, Virginia 20153-1200
Telephone No: (703) 766-3701
Facsimile No: (703) 766-3644

MLF/SWN:dlg